O.P.Code: 23CS0506	R23	H.T.No.									

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech. II Year II Semester Regular & Supplementary Examinations March/April-2026

DIGITAL LOGIC AND COMPUTER ORGANIZATION

(Common to CSM, CAD & CAI)

Time: 3 Hours **Max. Marks: 70**

PART-A

(Answer all the Questions **10 x 2 = 20** Marks)

1	a	What are the basic properties of Boolean algebra?	CO1	L2	2M
	b	List out the names of basic logical operators.	CO1	L1	2M
	c	What is Flipflop and different types of Flipflop?	CO2	L1	2M
	d	Sketch the basic functional units of computer.	CO2	L2	2M
	e	What is the advantage of using Booth algorithm?	CO3	L2	2M
	f	What are the basic operations to execute a complete instruction?	CO3	L2	2M
	g	Classify main memory and secondary memory.	CO4	L2	2M
	h	Define virtual memory.	CO4	L1	2M
	i	What are the examples of processor?	CO5	L1	2M
	j	What is the need of buses and classify the bus structure?	CO5	L2	2M

PART-B

(Answer all Five Units **5 x 10 = 50** Marks)

UNIT-I

2	a	Simplify the given Boolean expression using K-map F(A,B,C,D)= Σm(0,2,3,8,10,11,12,14).	CO1	L3	5M
	b	Define combinational circuit and explain the procedure for designing a combinational circuit.	CO1	L2	5M

OR

3	a	Explain about Binary Half Adder with truth table and logic diagram.	CO1	L2	5M
	b	Define Decoder and explain in detail about a 2-to-4-line binary decoder.	CO2	L2	5M

UNIT-II

4	a	Explain the working principle of SR and JK flip-flops	CO2	L2	5M
	b	Explain in detail about 3-bit ripple Up-counter using suitable diagram.	CO2	L2	5M

OR

5	a	Give the Structure of BUS Interface with various devices in computer.	CO3	L4	5M
	b	Explain briefly about the software of a computer.	CO3	L3	5M

UNIT-III

6	a	Explain the multiple bus organization.	CO4	L2	5M
	b	Differentiate between Hardwired Control and Micro-programmed control.	CO4	L2	5M

OR

7		Develop flowchart for the Multiplication of floating-point number and illustrate with an example.	CO5	L2	10M

UNIT-IV

8	a	What is cache memory? What is hit and miss in the cache memory.	CO5	L3	6M
	b	List and explain different mapping in Cache memory.	CO1	L3	4M

OR

9	a	Describe in detail about the memory management requirements.	CO1	L2	5M
	b	Compare various types of secondary storage systems.	CO1	L2	5M

UNIT-V

10	a	Explain the interrupt Nesting.	CO2	L3	5M
	b	Explain about interrupt service routine (ISR).	CO2	L2	5M

OR

11		Draw the USB architecture and explain it.	CO3	L2	10M

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